FLASH MEMORY CELL ARRAYS HAVING DUAL CONTROL GATES PER MEMORY CELL CHARGE STORAGE ELEMENT

ABSTRACT OF THE DISCLOSURE

A flash NAND type EEPROM system with individual ones of an array of charge storage elements, such as floating gates, being capacitively coupled with at least two control gate lines. The control gate lines are preferably positioned between floating gates to be coupled with sidewalls of floating gates. The memory cell coupling ratio is desirably increased, as a result. Both control gate lines on opposite sides of a selected row of floating gates are usually raised to the same voltage while the second control gate lines coupled to unselected rows of floating gates immediately adjacent and on opposite sides of the selected row are kept low. The control gate lines can also be capacitively coupled with the substrate in order to selectively raise its voltage in the region of selected floating gates. The length of the floating gates and the thicknesses of the control gate lines can be made less than the minimum resolution element of the process by forming an etch mask of spacers.

BEST AVAILABLE COPY